A Study of Parasitic Effects of ESD Protection on RF ICs

Ke Gong, *Member, IEEE*, Haigang Feng, *Student Member, IEEE*, Rouying Zhan, and Albert Z. H. Wang, *Senior Member, IEEE*

***Abstract*—This paper presents a comprehensive study on influences of on-chip electro-static discharge (ESD) protection structures on performance of the circuits being protected. Two novel compact low-parasitic ESD structures were designed for RF and mixed-signal (MS) integrated circuits. Parasitic models of the ESD structures are extracted. RF building-block circuits, including a low-power high-speed op amp and a fully integrated 2.4-GHz low-noise amplifier were designed in 0.18/0.35-μm technologies. Investigation of performance of these circuits under influences of the two new ESD protection structures and traditional MOS ESD protection device, in both copper and aluminum interconnects, demonstrated that significant circuit performance degradation ($\sim$30%) occur when using NMOS ESD protection in Al technology, which recovered substantially ($\sim$80%) when using low-parasitic ESD protection in Cu technology. This work indicates that the ESD-to-circuit influence is inevitable and substantial. Therefore, novel low-parasitic ESD protection solution is essential to maintaining both circuit functionality and ESD robustness in RF and MS applications.**

***Index Terms*—Electrostatic discharge, ESD parasitic, ESD protection, LNA, noise, RF.**

I. Introduction

ON-CHIP electro-static discharge (ESD) protection design becomes a major challenge in high-frequency and very deep submicrometer (VDSM) integrated circuit (IC) design due to ESD-induced parasitic effects and silicon consumption of ESD protection structures. The main ESD protection design tradeoff in advanced RF and mixed-signal (MS) applications is to achieve high ESD protection level (beyond 4 kV) and to maintain very low parasitic effects that exist in all ESD protection units. Such inevitable ESD-induced parasitic effects include parasitic *RC* delay (ESD capacitance, $C_{\rm ESD}$, and resistance) and noises (both substrate noise coupling due to $C_{\rm ESD}$, not considered in this paper, and ESD self-generated noises, focus of this paper), which are usually ignored in IC designs. However, these ESD-induced parasitic effects and the large size consumed by ESD protection units may be killing factors for RF and MS ICs in the VDSM regime. Traditional MOS-based ESD protection structures are not suitable to RF applications because of their big size, large $C_{\rm ESD}$, and strong noise contribution. It is, therefore, imperative to develop novel compact low-parasitic ESD protection structures and to thoroughly investigate the negative impacts of ESD protection on-chip performance, thereafter referred to as ESD-to-circuit influence [1].

In this paper, two novel compact low-parasitic ESD protection structures are introduced. A comparison study of the complex ESD-to-circuit influences using conventional MOS ESD protection structure and the two new ESD protection designs will be discussed for several RF building blocks. The new ESD protection structures are described in Section II, with related ESD parasitic models being introduced in Section III. Section IV discusses design of a low-power high-speed op amps circuit and a fully integrated 2.4-GHz low-noise amplifier (LNA) circuit, chosen for broad range circuit functionality comparison. Section V discusses overall ESD-to-circuit influences. Section VI presents concluding remarks.

II. ESD Protection Structures

Two novel compact low-parasitic ESD protection structures were designed for parasitic and area sensitive RF and MS applications. In order to perform meaningful ESD-to-circuit comparison studies, both the two new ESD protection structures and traditional MOS-based ESD protection units were used in this study. For equivalent comparison, all ESD protection structures used in this study targeted for the same ESD protection level of 4 kV in the human body model (HBM). Design of various ESD protection structures were conducted using a mixed-mode ESD simulation-design methodology for design prediction in this paper [2].

A. Complete ESD Protection Schemes

A complete full-chip ESD protection scheme is illustrated in Fig. 1, where each bond pad requires proper ESD protection. The ESD protection principle is to establish an efficient shunt path between each pair of bond pads to safely discharge ESD transients. The ESD protection structure placed at bond pads must be able to protect the chip against ESD transients of all modes [3], [4], i.e., I/O-to-V_{DD} positively (PD) and negatively (ND), I/O-to-ground (GND or V_{SS}) positively (PS) and negatively (NS), as well as from V_{DD}-to-GND (DS). In multi-supplies cases, ESD devices are also required between power buses of different levels. Clearly, in cases of big ESD protection devices being used for high ESD protection or a large number of ESD protection units needed in high pin-count applications, one would encounter significant ESD-induced parasitic effects.

Manuscript received April 27, 2001.

K. Gong was with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL 60616 USA. He is now with Agere Systems Inc., Allentown, PA 18109 USA.

H. Feng, R. Zhan, and A. Z. H. Wang are with the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, IL 60616 USA (e-mail: awang@ece.iit.edu).

Publisher Item Identifier S 0018-9480(02)00848-7.

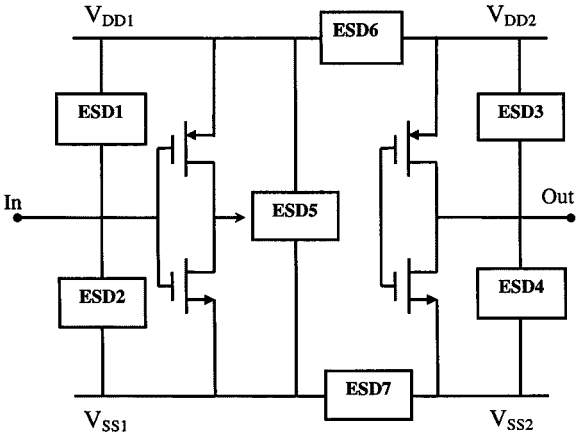

Fig. 1. Full-chip ESD protection diagram.

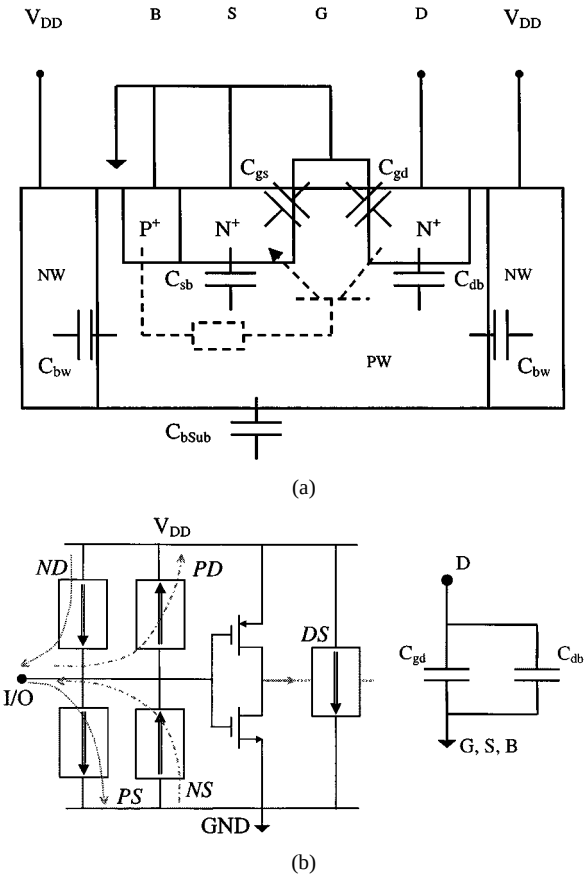

Fig. 2. ESD1: a traditional GGNMOS ESD protection structure. (a) Cross section. (b) Complete ESD protection scheme—four devices may be needed for an I/O pad. (c) ESD parasitic capacitance model.

B. MOS ESD Protection

Fig. 2(a) illustrates a classic NMOS ESD protection structure in grounded-gate (GGNMOS) format [5], referred to as ESD1 in this paper, where the drain (D) is connected to an I/O pad and the source (S), and gate (G) and body (B) are shortened together to ground (GND). When a positive ESD pulse appears at the I/O pin, the DB junction is reverse biased until breakdown occurs, where the generated hole current flows into GND via the body contact. Since S and B contacts are shortened, a positive BS PN junction voltage builds up to its forward turn-on

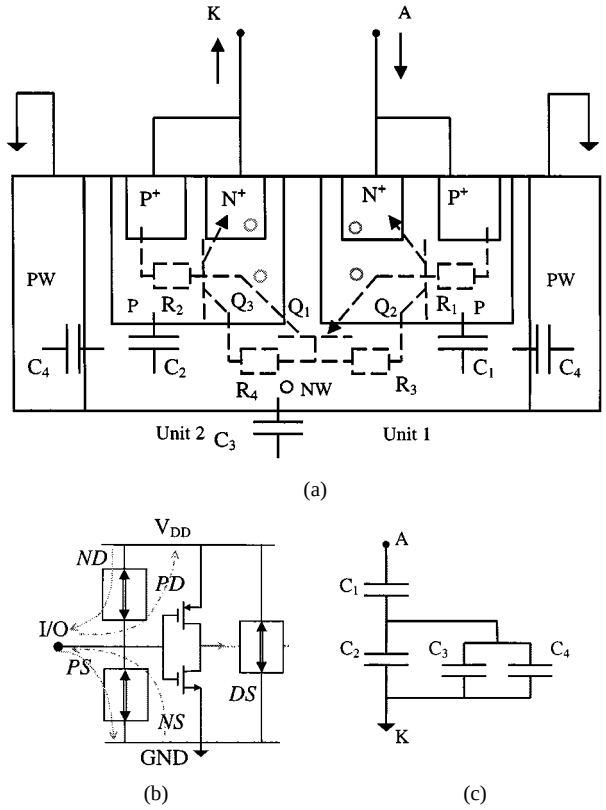

Fig. 3. ESD2: a new dual-direction ESD protection structure. (a) Cross section. (b) Complete ESD protection scheme—two devices may be needed for an I/O pad. (c) ESD parasitic capacitance model.

point and triggers the parasitic lateral NPN transistor. Hence, a low-impedance shunt path forms to discharge the ESD transient safely. To realize ESD protection level of 4 kV in HBM test model, a four-finger GGNMOS structure of equivalent length of 200 μm, with each finger of 50-μm long, was designed for uniform performance, with data to be discussed in Section V. There are two main disadvantages for this NMOS structure. Firstly, It provides an active ESD discharge channel, using an NPN, in one direction only, and relies on parasitic shunt path for ESD protection in the opposite direction. In many cases, two ESD protection units may be needed between an I/O pin to V_{DD} (V_{SS} as well) for complete ESD protection, as depicted in Fig. 2(b). Secondly, it usually has a large size for high ESD protection. Therefore, along with multi-ESD devices needed for each pin, it produces significant ESD parasitic effects and consumes a large amount of silicon.

C. A New Dual-Direction ESD Protection Structure

To address the above inefficiency of MOS ESD protection, a new dual-direction ESD protection structure was designed, with its cross section illustrated in Fig. 3(a), referred to hereafter as ESD2. Briefly, it is a two-terminal (A and K) five-layer ($NPNPN$, marked with gray circles) structure consists of one lateral PNP transistor (Q_1), two vertical NPN transistors (Q_2 and Q_3) and parasitic resistors (R_1, R_2, R_3, and R_4). The structure is connected to form two functional silicon-controlled rectifier (SCR) units (unit 1 of Q_1, Q_2, R_1, and R_3, and unit 2 of Q_1, Q_3, R_2, and R_4) with A and K being the electrodes. In operation, when a positive ESD pulse appears at electrode A with

respect to K, BC junction (NP) of Q_1 is reverse biased to its breakdown and the generated holes are collected by the negative terminal K via the P^+ contact layer. Since both the P^+ and N^+ contact layers are connected to K, V_{BE} (PN) of Q_3 increases and eventually turns on Q_3. The SCR unit 2 (left-hand side) is, therefore, triggered off (at V_{t1}) and driven into deep snapback region (holding voltage $V_h \leq 2$ V). An *active* discharge path with negligible impedance R_{ON} is thereby formed to shunt the huge ESD current surge and to clamp the I/O pad to a sufficient low-voltage level ($V_h \leq 2$ V), thus protects the ICs from being ESD damaged. After the ESD pulse is over, the thyristor quickly discharges and then turns off as the current decreases to below its holding current level (I_h). Similarly, the SCR unit 1 (right-hand side) operates during a negative ESD pulse event (K with respect to A). Hence, this structure forms a dual-direction ESD protection device to actively discharge ESD transients in both directions. In addition, the deep snapback I–V characteristic ensures very high ESD surge handling capacity. A small size of a 50-μm-long device was sufficient for 4-kV HBM ESD protection, with data to be discussed in Section V. Therefore, for complete ESD protection at each I/O pin, only two small ESD protection units are needed, each from I/O to V_{DD} and V_{SS} (GND), as illustrated in Fig. 3(b), as oppose to four large GGMOS ESD protection devices. In addition, a power clamp unit is needed for DS-mode ESD protection.

D. New All-Direction ESD Protection Structure

As discussed previously, two dual-direction units are still needed for each pad to achieve complete ESD protection. As an improvement, a new all-in-one ESD protection structure was devised. As depicted in Fig. 4(a), the new ESD protection structure, referred to as ESD3 in this paper, is a three-terminal (A, K_1, and K_2) device with eight functional layers ($NPNPNNPN$, marked by gray circles), consisting of six bipolar transistors (Q_1–Q_6) and parasitic resistors, which are electrically connected to form two dual-direction-type functional ESD2s. Unit I consists of lateral $Q_1 = PNP$, vertical $Q_2 = NPN$, and $Q_3 = NPN$, plus resistors. Unit II comprises lateral $Q_4 = PNP$, vertical $Q_5 = NPN$ and $Q_6 = NPN$. Q_3 and Q_5 share base and collector layers. R_2 and R_5 split the resistor of the central P region. A complete full-ESD protection scheme using this new all-in-one ESD protection structure is shown in Fig. 4(b), where its three electrodes, A, K_1 and K_2, are connected to I/O pin, i.e., V_{DD} and GND, respectively, on a chip. Operation of the all-in-one ESD protection structure is basically a dual-operation of the dual-direction ESD protection units. The structure is normally off. During ESD events, when ESD pulses appear at I/O pin with respect to V_{DD} (or GND), the Unit I (or Unit II) will function the same way as an ESD2 device does to provide adequate ESD protection correspondingly. Therefore, one single such structure provides full ESD protection for each pad against all four ESD stressing modes. In addition, extra unit (vertical NPN Q_2 and Q_6 + lateral PNP from $K1$ to $K2$) works as a power clamp for DS mode ESD protection between V_{DD} and ground. Hence, one single such structure serves as an all-in-one protection unit for each pad. In this paper, a small such device of 50 μm was adequate for 4-kV HBM ESD protection. Consequently, the ESD-induced parasitic effects and silicon consumption will be reduced substantially.

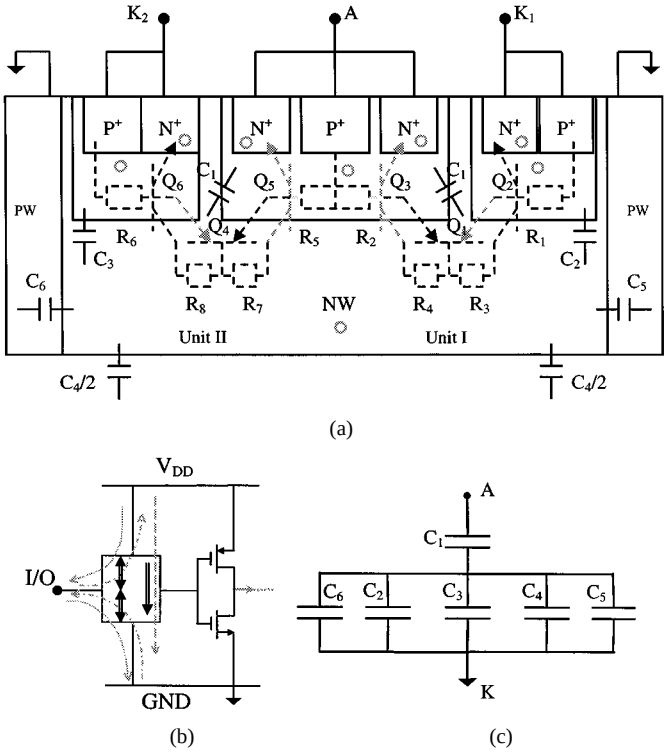

Fig. 4. ESD3: a new all-in-one ESD protection structure. (a) Cross section. (b) Complete ESD protection scheme—only one device needed for an I/O pad. (c) ESD parasitic capacitance model.

III. ESD Parasitic Modeling

Model extraction of these various ESD protection structures in this paper includes two parts: extracting ESD-induced parasitic capacitance $C_{\rm ESD}$ and modeling ESD-generated noises. The extracted ESD parasitic models were then used for circuit analyses.

A. Parasitic $C_{\rm ESD}$ Estimation

As mentioned previously, the same ESD compliance level (4-kV HBM) was targeted throughout this study to ensure meaningful comparison. Overall parasitic ESD capacitances $C_{\rm ESD}$ of each structure used consist of two portions, i.e., that associated with metal interconnect C_M and those originated in Si PN junctions, $C_{\rm Si}$. Hence, the total ESD capacitance of one protection structure will be $C_{\rm ESD} = C_{\rm Si} + C_M$. The $C_{\rm Si}$ for the three different ESD protection structures are discussed in Sections III-A.1–III-A.3, with the C_M being discussed in Section III-A.4.

1) Parasitic $C_{\rm Si}$ in ESD1 Structure: As depicted in Fig. 2(a), various parasitic junction capacitances (gate overlap capacitances $C_{\rm gd}$ and $C_{\rm gs}$, $D-B$ and $S-B$ capacitances C_{db} and C_{sb}, as well as body to substrate and n-well guard-ring capacitances $C_{b\rm Sub}$ and C_{bw}) are considered ESD1, e.g., GGNMOS. Considering the ESD protection operation condition for GGNMOS, where D is connected to an I/O pad, electrodes G, S, and B are grounded together, and n-well guard rings are connected to V_{DD}, as far as ac operation

is concerned, only the gate $C_{\rm gd}$ and reverse-biased C_{db} are significant. All others are negligible due to their forward or zero biasing. An equivalent parasitic network model is, hence, depicted in Fig. 2(c) for the GGNMOS. Straightforwardly, the total Si-originated ESD capacitance for a GGNMOS is given by $C_{\rm Si} = C_{\rm gd} + C_{db}$.

2) Parasitic $C_{\rm Si}$ in ESD2 Structure: The Si-originated parasitic capacitances in ESD2, e.g., the new dual-direction ESD protection structure, are extracted using the cross section shown in Fig. 3(a), where existing junction capacitances include C_1 and C_2 for the P-base/N-well junctions, C_3 for the N-well/substrate junction, and C_4 for N-well/P-well guard-ring junctions. Considering real ESD protection operation condition, where terminal A is connected to an I/O pad, while terminal K and P-well guard rings are grounded, as illustrated in Fig. 3(b), an equivalent ESD parasitic capacitance network model is extracted, as shown in Fig. 3(c). It is noteworthy that C_1 is included in the equivalent circuit due to dual-direction ESD protection consideration because C_1 is either positively or negatively biased for A-to-K or K-to-A ESD stresses. Hence, its total Si-originated ESD capacitance is given by

$$C_{\rm Si} = \frac{C_1(C_2 + C_3 + C_4)}{C_1 + C_2 + C_3 + C_4}.$$

3) Parasitic $C_{\rm Si}$ in ESD3 Structure: As illustrated in Fig. 4(a), Si-originated ESD parasitic capacitances in ESD3, e.g., the new all-in-one ESD protection structure, include C_1 of the P-base/N-well junction for A, C_2, and C_3 for the P-base/N-well junctions for $K1$ and $K2$, C_4 for the N-well/substrate junction, as well as C_5 and C_6 for N-well/P-well guard-ring junctions. Considering its dual-direction ESD protection mechanisms between any pair of three terminals (A, $K1$ and $K2$), its equivalent ESD parasitic capacitance network in the ac mode is depicted in Fig. 4(c). The total Si-originated ESD capacitance can be written as

$$C_{\rm Si} = \frac{C_1(C_2 + C_3 + C_4 + C_5 + C_6)}{C_1 + C_2 + C_3 + C_4 + C_5 + C_6}.$$

4) Parasitic C_M of ESD Metal Interconnect: ESD-induced parasitic capacitances associated with ESD protection metal interconnect C_M cannot be ignored in high-density IC design, which were included into the total $C_{\rm ESD}$ consideration, along with the Si-originated $C_{\rm Si}$, in this study. A commercial six-metal 0.18-μm CMOS technology was used in this study. An integrated mixed-mode ESD simulation-design methodology [6] was used in this study, where metal interconnect reliability was included into ESD design simulation with multilevel coupling (process–device–circuit–electronic–thermal) to predict ESD protection performance. Overall consideration of C_M has two folds. Firstly, C_M exists generally in any ESD protection structures. In this study, ESD protection metal interconnect mainly uses metal layers 1 and 2 ($M1$ and $M2$) following the design rules, with $M1$ for primary ESD protection device coverage and $M2$ for routing bridges. Study of the layout suggests that the main source of parasitic C_M comes from ESD metal lines associated with inter-layer capacitances, including metal-to-substrate, inter-metals, as well as metal-to-poly-gate, i.e., C_{MF} for $M1$-to-substrate over field, C_{MD} for $M1$-to-diffusion, C_{MP} for $M1$-to-Poly 1, and C_{MM} for $M1$-to-$M2$. Material data, such as inter-layer dielectric thickness and permittivity (ε), for the process used are listed in Table I. Secondly, comparison for using Cu and Al interconnect technologies was included in this study. The rationale follows. ESD design simulation in this study found that Cu is superior to Al in ESD protection toughness. Alternatively, to achieve the same level of ESD protection, (i.e., 4 kV in this paper), much less Cu metal ESD coverage was needed compared to that in using a traditional Al interconnect, which translates into fewer ESD-induced parasitic capacitances due to less ESD metal coverage [1], [7]. Specifically, this study found that around 30% of ESD metal coverage reduction was realized in using Cu compared to Al, as illustrated by the data shown in Table II.

TABLE I
INTER-LAYER DIELECTRIC THICKNESS AND PERMITTIVITY DATA FOR $C_{\rm ESD}$ ESTIMATION IN A 0.18-μm CMOS TECHNOLOGY

From	To	Thickness (KÅ)
Metal 1	Diffusion	10
Metal 1	Substrate	14
Metal 1	Poly-1	8
Metal 1	Metal 2	5.7
ILD-layers	ILD-films	ε
STI	SiO2	3.6
ILD	Si3N4	7
MD1	SiO2	3.6

TABLE II
ESTIMATED $C_{\rm Si}$ AND C_M FOR 4-kV FULL ESD PROTECTION

Structures	ESD1		ESD2		ESD3	
C_{Si} (pF)	0.54		0.09		0.07	
C_M (pF)	Cu	Al	Cu	Al	Cu	Al
	0.30	0.43	0.029	0.041	0.019	0.028

5) Total Parasitic $C_{\rm ESD}$: Based upon the previous analyses on and models for the parasitic ESD capacitances, and assuming complete I/O ESD protection schemes depicted in Figs. 2(b), 3(b), and 4(b), the overall ESD-induced capacitances $C_{\rm ESD}$ can be estimated for all three different ESD protection structures (ESD1, ESD2, and ESD3) using the equation $C_{\rm ESD} = C_{\rm Si} + C_M$, where

$$\begin{aligned} C_{\rm Si} &= C_{\rm gd} + C_{db}, \qquad \text{for ESD1} \\ &= C_1 // (C_2 + C_3 + C_4), \qquad \text{for ESD2} \\ &= C_1 // (C_2 + C_3 + C_4 + C_5 + C_6), \qquad \text{for ESD3} \\ C_M &= C_{MD} + C_{MP} + C_{MF} + C_{MM} \end{aligned}$$

The modeled ESD capacitance data are summarized in Table II for $C_{\rm Si}$ and C_M, and in Table III for overall $C_{\rm ESD}$.

TABLE III
ESTIMATED $C_{\rm ESD}$ FOR 4-kV FULL ESD PROTECTION

Structures		ESD1	ESD2	ESD3
$C_{\rm ESD}$ (pF)	Al	0.10	0.13	0.97
	Cu	0.09	0.12	0.84

Several observations follow. First, sizable parasitic $C_{\rm Si}$ exists in the ESD1 protection structure, which was reduced substantially when using the two new ESD protection structures, i.e., ~83% reduction in ESD2 and a further ~22% decrease in ESD3 from ESD2. Secondly, considerable parasitic C_M was produced by ESD metal coverage in ESD1 in Al technology. However, use of Cu technology significantly reduces such capacitance by an average 30%. Thirdly, the overall $C_{\rm ESD}$ was greatly reduced when using the compact ESD2 (~85%) and ESD3 (~89%) compared to the traditional ESD1 structure. The benefits of the reduction in $C_{\rm ESD}$ to general RF and MS circuit performance will be illustrated in Sections IV and V.

B. Noise Models for ESD Protection Structures

1) Noise Model for ESD1 Structure: Noise analysis of the ESD1, e.g., the GGNMOS ESD protection device, can be conducted based on MOSFET noise theory [8], [9], with the consideration that ESD1 is in an off state and its gate, source, and body are grounded together in ESD protection operation. The channel current I_D, which plays a main role in noise generation, is governed by the sub-threshold current equation [10]

$$I_D = K_1 \frac{W}{L} e^{(V_{GS}-V_{\rm th})/nV_T}\left(1 - e^{-V_{DS}/mV_T}\right)$$

where K_1 is a device-related parameter, $V_{\rm th}$ is the threshold voltage, V_T is the thermal voltage, n and m are the process factors (1~2), and W and L are MOSFET channel width and length, respectively. The dominating noise generators considered for ESD1 in ESD protection operation follow. The first one is channel resistance induced thermal noise $\overline{i_{nCh}}$ with its power spectrum density (PSD) given by [11], [12]

$$\overline{i_{nCh}^2} = 4kT\gamma g_m \Delta f$$

where k is the Boltzmann's constant, T is the absolute temperature, $\gamma \geq 2-3$ is for a short-channel device (≈1 for a long-channel at $V_{DS} = 0$), and Δf is the bandwidth. The transconductance g_m is given by

$$\begin{aligned} g_m &= \frac{\partial I_D}{\partial V_{GS}} \\ &= \frac{K_1 W}{nV_T L} e^{(V_{GS}-V_{\rm th})/nV_T}\left(1 - e^{-V_{DS}/mV_T}\right) \\ &= \frac{I_D}{nV_T}. \end{aligned}$$

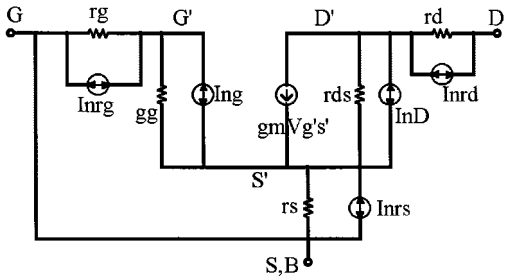

Fig. 5. Model circuit for ESD-induced noises: ESD1.

The second noise generator is flicker noise ($\overline{i_{nf}}$) due to surface defects, as depicted by [11], [12]

$$\overline{i_{nf}^2} = \frac{K_2 I_D^{\alpha_f}}{fC_{\rm ox}L_{\rm eff}^2}\Delta f$$

where α_f is a flicker noise constant (0.5~2), K_2 is a device-specific coefficient, $C_{\rm ox}$ is unit gate–oxide capacitance, and $L_{\rm eff}$ is effective channel length. Hence, the total channel current generated noise $\overline{i_{nD}}$ is given by

$$\overline{i_{nD}^2} = \overline{i_{nCh}^2} + \overline{i_{nf}^2} = 4kT\gamma g_m \Delta f + \frac{K_2 I_D^{\alpha_f}}{fC_{\rm ox}L_{\rm eff}^2}\Delta f.$$

The third noise source is the induced-gate noise $\overline{i_{ng}}$ associated with fluctuation in gate leakage current due to coupling from the channel thermal noise, depicted by [11], [12]

$$\overline{i_{ng}^2} = \frac{16}{15} kT\delta\omega^2 C_{\rm gs}^2 \Delta f$$

where $C_{\rm gs} = (2/3)C_{\rm ox}WL$, and δ is determined by the channel length. This type of noise becomes significant in high-frequency applications, such as RF integrated circuits (RF ICs). A fourth noise generator considered is related to distributed gate resistance r_g, as given by

$$\overline{i_{nrg}^2} = \frac{4kT}{3r_g}\Delta f$$

where a factor of 1/3 is included for a distributed transmission-line effect in high frequency. In addition, thermal noise sources associated with series drain and source resistances r_d and r_s are given as

$$\overline{i_{nrd}^2} = \frac{4kT\Delta f}{r_d}$$

and

$$\overline{i_{nrs}^2} = \frac{4kT\Delta f}{r_s}.$$

Other minor noise sources, such as gate shot noise, are negligible in ESD noise consideration. The extracted noise model for the ESD1 device is shown in Fig. 5, which is used in LNA circuit noise analysis, and is to be discussed in Section IV.

2) Noise Model for ESD2 Structure: Noise model for ESD2, e.g., the new dual-direction ESD protection structure, was developed based on bipolar junction transistor (BJT) noise theory [8]. Fig. 6 shows the equivalent circuit of the ESD2 device, which is in an off state under normal circuit operation. Major noise generators in ESD2 come from junction shot and flicker noises,

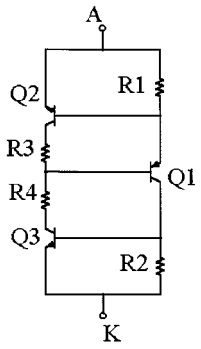

Fig. 6. Equivalent circuit for ESD2.

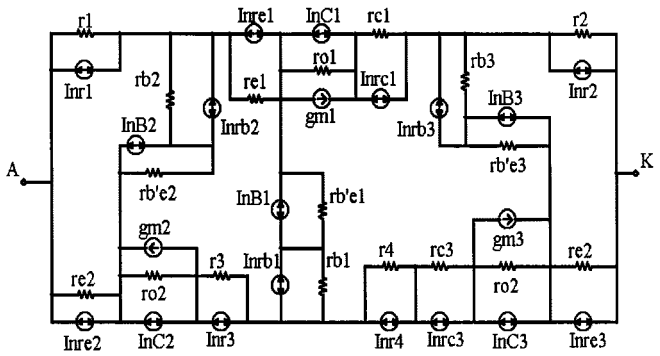

Fig. 7. Model circuit for ESD-induced noises: ESD2.

as well as series resistance thermal noises in each BJT. For the base–emitter (BE) junctions, the shot noises generators $\overline{i_{nB\text{shot}}}$ are given by [8], [11], [12]

$$\overline{i^2_{nB\text{shot}}} = 2qI_B\,\Delta f$$

and the flicker noises are in the format of [8], [11], [12]

$$\overline{i^2_{nBf}} = \frac{K_2 I_B^{\alpha_f}}{f}\,\Delta f$$

where I_B is the base current. Hence, the total BE junction noises are

$$\overline{i^2_{nB}} = \overline{i^2_{nB\text{shot}}} + \overline{i^2_{nBf}} = 2qI_B\,\Delta f + \frac{K_2 I_B^{\alpha_f}}{f}\,\Delta f.$$

For the base–collector (BC) junctions, flicker noises are negligible and the total junction noises dominated by shot noises are given by [8], [11], [12]

$$\overline{i^2_{nC}} = \overline{i^2_{nC\text{shot}}} = 2qI_C\,\Delta f$$

where I_C is the collector current. In addition, thermal noises generated by BJT series resistances r_c, r_e, and r_b, as well as parasitic resistances ($R = R1 - R4$), are given by

$$\overline{i^2_{nrc}} = \frac{4kT\,\Delta f}{r_c}$$
$$\overline{i^2_{nre}} = \frac{4kT\,\Delta f}{r_e}$$
$$\overline{i^2_{nrb}} = \frac{4kT\,\Delta f}{r_b}$$
$$\overline{i^2_{nR}} = \frac{4kT\,\Delta f}{R}.$$

The complete noise model for the ESD2 device is depicted in Fig. 7, which was used in LNA circuit analysis.

3) Noise Model for ESD3 Structure: Extraction of the noise model for ESD3, e.g., the new all-in-one ESD protection, is similar to that of ESD2 because functionally ESD3 comprises two ESD2, as shown in Fig. 4(a). Individual noise generators associated each BJT junction can be extracted following the procedures used for ESD2, and a noise circuit model was extracted, of course, in a more complex format. It is noteworthy that overall noise generation in ESD3 is reduced compared to using two ESD2 for an I/O pad because vertical $NPN\ Q_3$, and Q_5, as well as R_2 and R_5 in the central P region are shared by the two functional units in ESD3. Such reduction in overall ESD-induced noises was observed in LNA circuit analysis to be discussed in Section IV.

TABLE IV
OP-AMP CIRCUIT SPECIFICATIONS

Technology	0.18um, 3V, Cu, 1P6M
Gain (dB)	73.07
Phase margin	70.1°
f_T (MHz)	120.7
f_{-3dB} (kHz)	29.7
V-swing (V, @80%)	0.96
Settling time (ns, @1%)	3.77
SR (mV/ns)	115.9
Power cons. (mW)	0.43

IV. CIRCUIT DESIGN AND CONSIDERATION

Aiming to study the comprehensive ESD-to-circuit influences, two RF circuits were chosen and designed in this study. A high-speed op amp was used to evaluate ESD negative impacts on general circuit functionalities and an LNA circuit was used for ESD-added noise analysis.

A. Op-Amp Circuit

To illustrate the whole-spectrum influences of the ESD parasitic C_{ESD} on the circuits, a low-power high-performance op amp was designed and used as a test vehicle in this study. The op-amp circuit, implemented in a commercial six-metal 0.18-μm 3-V CMOS technology, features low power (0.43 mW), high slew rate (116 mV/ns), short settling time (3.7 ns at 1%), wide output swing (0,96 V at 80% gain), and large unity-gain bandwidth (121 MHz), as summarized in Table IV. Fig. 8 shows the op-amp schematic consisting of a differential pair input stage for better noise rejection; a source–follower gain stage for high gain and level shift, a class-AB complementary push–pull output stage with low quiescent current for high-swing low-power consumption, as

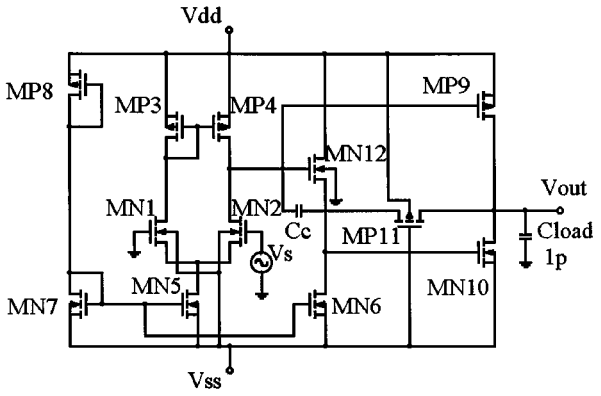

Fig. 8. Schematic for the op-amp circuit.

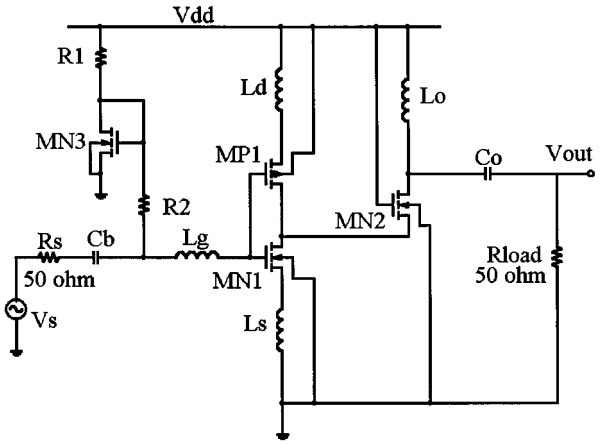

Fig. 9. Schematic for the LNA circuit.

well as crossover distortion elimination, and a compensation capacitor C_C with an active nulling resistor for wide bandwidth and adequate stability. ESD-induced parasitic $C_{\rm ESD}$ in the full ESD protection case using ESD1, ESD2, and ESD3 protection structures was included in circuit analysis and simulation. The impact of $C_{\rm ESD}$ on the circuit performance is discussed in Section V.

B. 2.4-GHz LNA Circuit

An LNA circuit was used in this study to investigate the impacts of ESD-self-generated noises on circuit noise performance. This fully integrated LNA circuit is shown in Fig. 9 and features a two-stage topology to realize high gain. A current sharing scheme was used in biasing to ensure low power consumption. On-chip inductors and an inductive source degeneration technique were used for on-chip impedance matching (50 Ω) at both input and output ports. The LNA circuit was implemented in a commercial four-metal 0.35-μm 3-V CMOS technology. Typical circuit specifications include frequency of a 2.4-GHz noise figure (NF) of 1.76 dB and very low power consumption of 24 mW, as summarized in Table V. ESD noise models for the three ESD protection structures, developed in Section III, were included in evaluating ESD noise impacts on circuit noise performance, with the results to be discussed in Section V.

TABLE V
LNA CIRCUIT SPECIFICATIONS

Center freq. (GHz)	2.41 GHz
S21 (dB)	23.4
S11 (dB)	-34.5
S22 (dB)	-47.7
S12 (dB)	-39.6
Power supply (V)	3
Current (mA)	8.52
Noise figure (dB)	1.76

TABLE VI
DATA FOR ESD PROTECTION STRUCTURES USED

ESD devices	Methods	Triggering V_{t1} (V)	Holding V_h (V)	R_{ON} (Ω)
ESD1	Simulation	14.68	6.92	~1.9
	C-tracer	12.56	6.48	-
	TLP	12.5	6.5	~1.02
ESD2	Simulation	23.32	1.58	0.73
	C-tracer	22.8	1.55	-
	TLP	21.75	2.96	1.4
ESD3	Simulation	20.82	1.31	0.5
	C-tracer	22.5	1.5	-
	TLP	21.66	2.41	1.37

ESD type	ESD pass level		Simulated ESD device triggering time t_1 (nS)
	Simulation	HBM Test	
ESD1, 200μ	4KV	4KV	0.2
ESD2, 50μ	4KV	4KV	0.18
ESD3, 50μ	4KV	4KV	0.16

V. RESULTS AND DISCUSSIONS

A. Results of ESD Protection Structures

The ESD protection structures used in this study were designed using an integrated mixed-mode ESD simulation-design approach for design prediction [2], [6]. For meaningful comparison, a same 4-kV HBM ESD protection level was adopted. ESD measurements include quasi-dc tests by a curve tracer, transient tests by a transmission-line-pulsing (TLP) tester, and standard HBM zapping tests. Typical simulation and test data are summarized in Table VI. Fig. 10 shows a typical dual-direction I–V characteristic for an ESD3 structure ($A-K1$) by a curve tracer. The desired dual-direction deep-snapback low-impedance active discharge channel was clearly observed from this graph. Standard ESD zapping test shows that all ESD structures pass 4-kV HBM stresses.

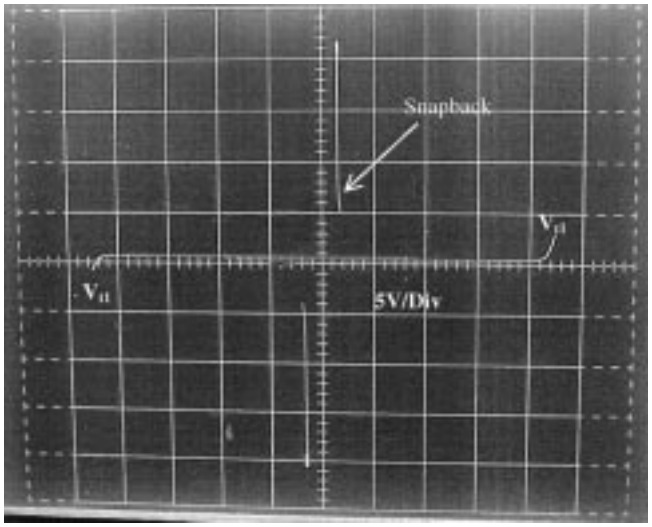

Fig. 10. Measured I–V curve for an ESD3 structure.

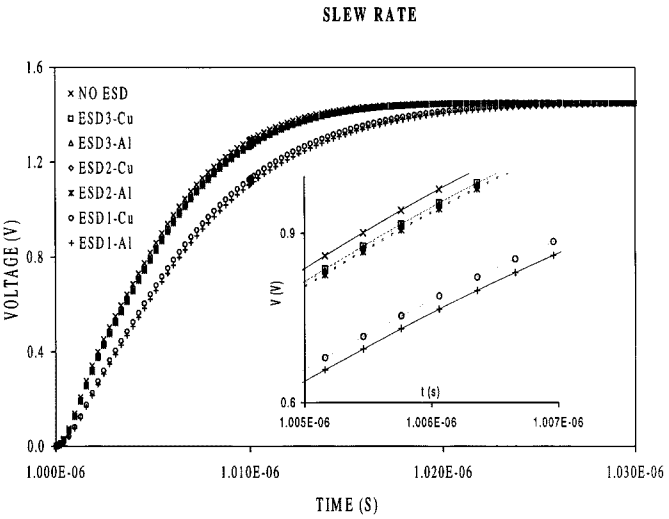

Fig. 12. Large-signal response of the op-amp circuit without and with ESD protection (ESD1, ESD2, and ESD3) in both the Cu and Al interconnect.

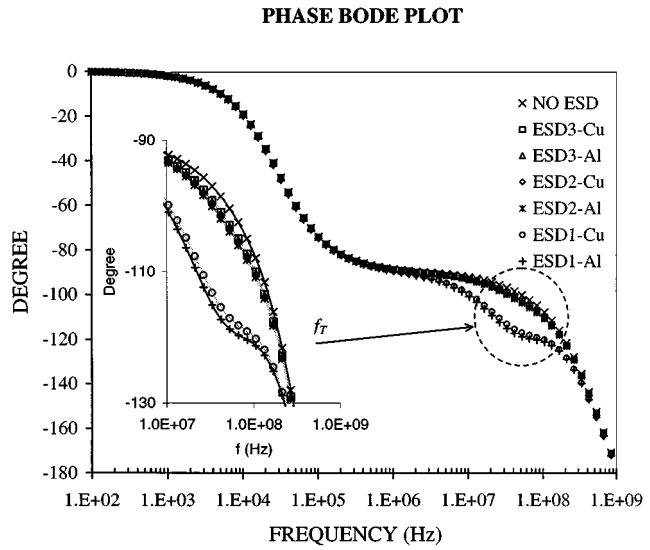

Fig. 11. Phase bode plot of the op-amp circuit without and with ESD protection (ESD1, ESD2, and ESD3) in both Cu and Al interconnects.

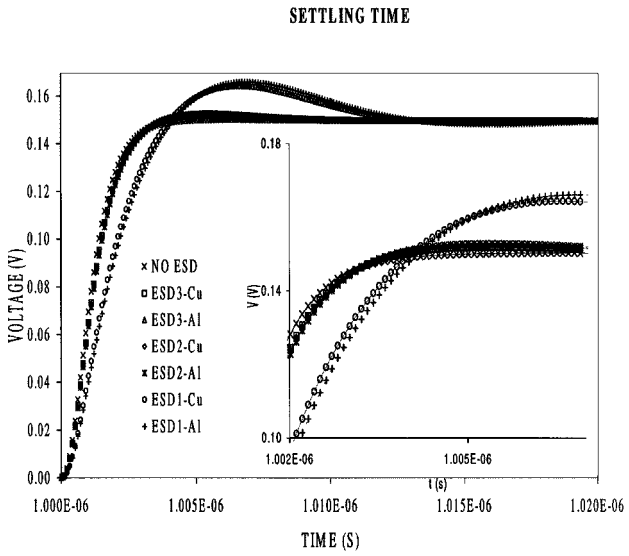

Fig. 13. Small-signal response of the op-amp circuit without and with ESD protection (ESD1, ESD2, and ESD3) in both the Cu and Al interconnect.

B. C_{ESD}-to-Circuit Influences on Op Amp Circuit

Figs. 11–13 show typical performance graphs for the high-performance op-amp circuit, implemented in a commercial six-metal 0.18-μm CMOS technology using both Cu and Al interconnects, i.e., a phase Bode plot, a large-signal step response for a slew-rate test, and a small-signal step response for settling time extraction. Circuit performance—the C_{ESD}-to-circuit impacts—was evaluated for the op-amp circuit without and with ESD protection, using ESD1, ESD2, and ESD3 structures in both Cu and Al interconnects. A detailed comparison in circuit specifications can be drawn from the typical data listed in Table VII. For example, the unity-gain bandwidth f_T reduces 38.7% when using ESD1 in Al, however, use of compact ESD2 and ESD3 recovers the lose substantially, i.e., by 81%. The phase margin reduces by 14% when using ESD1 in Al, which was recovered by 89% in using ESD3. Most critical circuit specifications suffer degradation when using the large-size ESD1 structure, which was significantly recovered by using compact ESD2 and ESD3 protection. Further, more improvement was observed in circuits using a new Cu interconnect due to even less ESD-metal-induced capacitances. A detailed data comparison is summarized in Table VIII. The results clearly show that ESD-induced parasitic capacitances are becoming intolerable to high-performance RF and MS ICs, and compact robust ESD protection solution are highly desirable in avoiding such circuit performance degradation while maintaining adequate ESD protection.

C. ESD Noise Impacts on LNA Circuit

Generally, there are two types of noise effects associated with ESD protection structures: the first one, the commonly understood substrate noise coupling via C_{ESD}, which can be evaluated by injecting noise signals into GND pads, was not considered in this study; the second one, largely overlooked, is the ESD-self-generated noises, which is directly related to the features and sizes of ESD protection structures used. The latter

TABLE VII
C_{ESD}-TO-OP-AMP INFLUENCES USING DIFFERENT ESD PROTECTION STRUCTURES ($C_L = 1$ pF)

		f_T (MHz)	Phase Margin	Slew Rate (mV/ns)	Settling Time (ns)
No ESD		120.7	70.1°	115.9	3.77
ESD1	Al	74.0	60.0°	81.0	17.07
	Cu	77.5	61.2°	84.4	11.92
ESD2	Al	109.9	68.7°	109.9	7.60
	Cu	110.7	68.8°	110.4	7.47
ESD3	Al	112.2	69.0°	111.1	7.15
	Cu	113.0	69.1°	111.5	6.85

TABLE VIII
COMPARISON OF C_{ESD}—CAUSED PERFORMANCE DEGRADATION OF OP-AMP CIRCUIT IN Al INTERCONNECT

Parameters	No C_{ESD}	ESD1	ESD2	ESD3
f_T (MHz)	120.7	-38.7%	-8.9%	-7.0%
		Recovery		
		→ + 81.9% (+83.5% in Cu) →		
Phase Margin	70.1°	-14.4%	-2.0%	-1.6%
		Recovery		
		→ + 88.9% (+90.3% in Cu) →		
Slew rate (mV/ns)	115.9	-30.1%	-5.2%	-4.1&
		Recovery		
		→ + 86.4% (+88.7% in Cu) →		
t_{set} (ns, 1%)	3.77	-353%	-102%	-89.7
		Recovery		
		→ +74.6% (+76.9% in Cu) →		

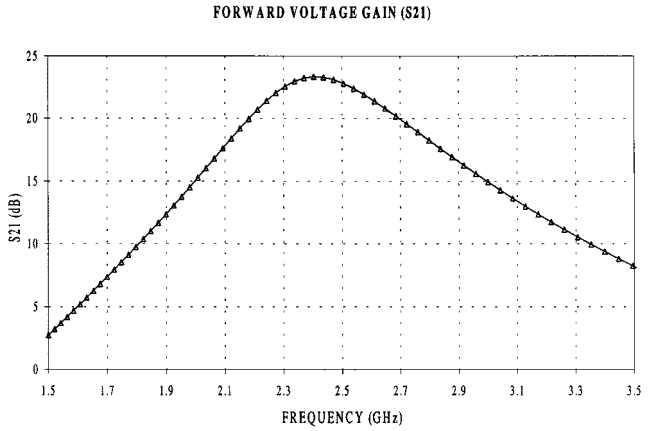

Fig. 14. S_{21} of the LNA circuit.

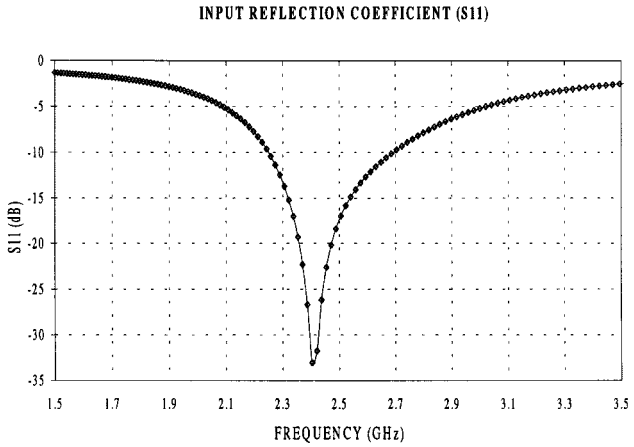

Fig. 15. S_{11} of the LNA circuit.

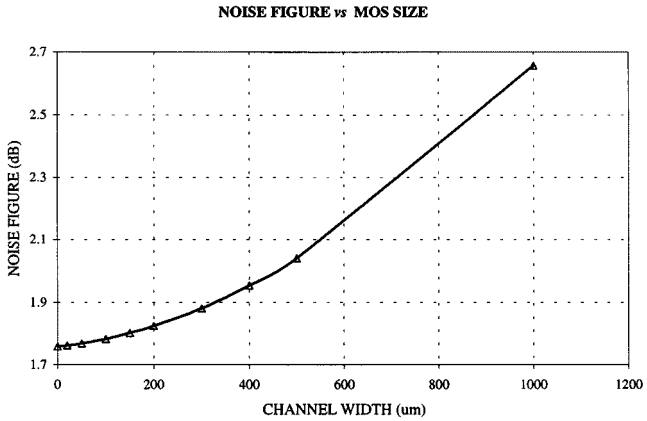

Fig. 16. NF of the LNA circuit using ESD1 protection with different sizes shows dependence of the LNA NF on ESD-induced noises.

TABLE IX
ESD NOISES TO LNA INFLUENCES

ESD Type	NF (dB)	Degradation
No ESD	1.7582	-
ESD1	1.8247	3.78%
ESD2	1.7596	0.08%
ESD3	1.7586	0.02%

ESD noise impact was the focus of this study. Typical S-parameter plots for the LNA circuit, implemented in a commercial four-metal 0.35-μm dual-poly CMOS technology, are shown in Figs. 14 and 15, with critical data listed in Table V. The LNA features include S_{21} of 23.4 dB at the center frequency of 2.41 GHz and an NF of 1.76 dB. The total current is 8.52 mA at 3-V operation, which is much lower than that reported [13]–[15] with a similar supply voltage. Comprehensive evaluation of ESD-self-generated noise contribution to the LNA circuit was conducted for circuits using ESD1, ESD2, and ESD3 protection structures. Fig. 16 shows the relationship between the LNA NF and ESD protection device sizes using ESD1 (hence, different ESD-induced noises), which clearly indicates the strong ESD-induced noise impact on overall LNA circuit noise performance. Data summarized in Table IX also demonstrate that a traditional GGNMOS (ESD1) structure has a noticeably worsened LNA NF (by 3.78%) due to its large ESD noise generation, while using compact ESD protection, (ESD2 and ESD3) almost totally recovered the degradation in noise performance (a mere 0.02% increase in the NF using ESD3). This implies that ESD-induced noises are not trivial when using conventional ESD protection structures and novel ESD protection solutions are essential to avoiding such circuit noise performance degradation while maintaining adequate ESD protection.

VI. Conclusions

In summary, this paper has presented a comprehensive study of the complex, however largely overlooked, ESD-to-circuit influences in ESD protection design for RF and MS applications. Two new low-parasitic ESD structures have been designed for RF ICs. A low-power high-speed op-amp circuit and a fully integrated 2.4-GHz LNA circuit have been designed and used as test vehicles to evaluate the complex ESD-to-circuit influences due to ESD-induced parasitic capacitances and noises using a classic MOS ESD protection and the two new ESD protection structures, all set for 4-kV ESD protection, including ESD-metal-induced parasitic effects in both Al and Cu interconnects. Models for ESD-induced capacitances and noises were proposed. The designs were implemented in commercial 0.18- and 0.35-μm CMOS technologies. Results show that, when using large-size MOS ESD protection, its parasitic capacitances may cause significant performance degradation in the op-amp circuit, while ESD-self-generated noises increase the LNA NF substantially. Such performance degradation can be largely eliminated by using the new compact ESD protection structures. New Cu interconnect technology also reduces ESD-metal-related parasitic capacitances normally experienced in Al technology. This paper has indicated that the inevitable ESD-induced parasitic effects may have strong negative impacts on circuit performance. Low-parasitic compact ESD protection solutions are highly desirable both to eliminate the ESD-to-circuit influences and to reduce ESD-related Si consumption, particularly for RF and MS ICs in the VDSM regime.

Acknowledgment

The authors wish to thank United Microelectronics Corporation, China, and Asahi Kasei Microsystems Company, Japan, for using their CMOS process technologies.

References

[1] H. G. Feng, K. Gong, and A. Wang, "ESD protection design using copper interconnects: More robustness and less parasitics," SRC, Durham, NC, Pub. P000375, ser. Publications in copper design challenge, Mar. 17, 2000.

[2] A. Wang and C. Tsay, "A novel design methodology using simulation for on-chip ESD protection for ICs," in *Proc. IEEE 5th Int. Solid-State Integrated Circuits Technol. Conf.*, 1998, pp. 509–512.

[3] M. Ker, C. Wu, T. Cheng, and H. Chang, "Capacitor-couple ESD protection circuit for deep-submicron low-voltage CMOS ASIC," *IEEE Trans. VLSI Syst.*, vol. 4, pp. 307–321, Sept. 1996.

[4] S. Dabral and T. Maloney, *Basic ESD and I/O Design*. New York: Wiley, 1998.

[5] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*. New York: Wiley, 1995.

[6] H. G. Feng, K. Gong, and A. Wang, "A new integrated metal-semiconductor simulation methodology for on-chip electrostatic discharge protection design optimization," in *Proc. IEEE/IFIP World Comput. Congr.–Int. Conf. Design Automat.*, 2000, pp. 81–85.

[7] S. Voldmaan, G. Gauthier, D. Reinhart, and K. Morrisseau, "High-current TLP characterization of Al and Cu interconnects for advanced CMOS semiconductor technologies," in *Proc. IEEE Int. Rel. Phys. Symp. Dig.*, 1998, pp. 293–301.

[8] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling With SPICE*, 2nd ed. New York: McGraw-Hill, 1993.

[9] C. Enz and Y. Cheng, "MOS transistor modeling for RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, pp. 186–201, Feb. 2000.

[10] P. Wong, "MOSFET fundamentals," in *ULSI Devices*, C. Chang and S. Sze, Eds. New York: Wiley, 2000.

[11] P. Gray, P. Hurst, S. Lewis, and R. Meyer, *Analysis and Design of Analog Integrate Circuits*, 4th ed. New York: Wiley, 2001.

[12] T. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge, U.K.: Cambridge Univ. Press, 1998.

[13] D. Shaeffer and T. Lee, "A 1.5-V, 1.5-GHz CMOS low noise amplifier," *IEEE J. Solid-State Circuits*, vol. 32, pp. 745–759, May 1997.

[14] C. Kim, M. Park, C. Kim, Y. Hyeon, H. Yu, K. Lee, and K. Nam, "A fully integrated 1.9-GHz CMOS low-noise amplifier," *IEEE Microwave Guided Wave Lett.*, vol. 8, pp. 293–295, Aug. 1998.

[15] J. Rudell, J. Ou, T. Cho, G. Chien, F. Brianti, J. Weldon, and P. Gray, "A 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications," *IEEE J. Solid-State Circuits*, vol. 32, pp. 2071–2088, Dec. 1997.

Ke Gong (M'97) received the B.S.E.E. degree from the Tsinghua University, Beijing, China, in 1999, and the M.S.E.E. degree from the Illinois Institute of Technology, Chicago, in 2001.

He is currently with Agere Systems Inc. (formerly the Microelectronic Group, Lucent Technology), Allentown, PA, where he is an Integrated Circuit Designer. His research interests include analog, MS and RF IC designs, I/O cells, and ESD protection design.

Haigang Feng (S'00) received the B.S. degree in electrical engineering from the Tsinghua University, Beijing, China in 1998, the M.S. degree (with honors) in electrical engineering from the Illinois Institute of Technology, Chicago, in 2001, and is currently working toward the Ph.D. degree in electrical and computer engineering at the Illinois Institute of Technology.

His research concerns advanced ESD protection design for ICs, MS IC design, RFIC design, and system-on-chip design.

Rouying Zhan received the B.S. degree in electrical engineering from the Central South University, Changsha, China, in 1994, and the M.S. degree in electrical engineering from the University of Electronic Science and Technology, Sichuan, China, in 1997, and is currently working toward the Ph.D. degree in electrical engineering at the Illinois Institute of Technology, Chicago.

From 1997 to 2000, she was with the State Key Laboratory of Optical Fiber Transmission and Communication System, University of Electronic Science and Technology, where her research focused on telecommunication network management and network survivability. Her current research interests are IC computer-aided design (CAD) and ESD protection circuit and MS IC design.

Albert Z. H. Wang (A'95– M'97–SM'00) received the B.Eng. degree in electrical engineering from the Tsinghua University, Beijing, China, in 1985, the M.S. degree in electrical engineering from the Chinese Academy of Sciences, Shanghai, China, in 1988 and the Ph.D. degree in electrical engineering from the State University of New York at Buffalo, in 1995.

From 1995 to 1998, he was a Staff Research and Development Engineer at the National Semiconductor Corporation, Santa Clara, CA. In 1998, he joined the Department of Electrical and Computer Engineering, Illinois Institute of Technology, Chicago, as an Assistant Professor, and is currently the Director of the Integrated Electronics Laboratory. His research interests center on analog and MS ICs, RF CMOS ICs, low-power and low-voltage design, advanced on-chip ESD protection circuit simulation-design methodologies, very large scale integration (VLSI) CAD, system-on-chip (SoC) design, advanced semiconductor devices, etc. He has authored or co-authored over 45 journal and conference papers within these fields and *On-Chip ESD Protection for Integrated Circuits* (Norwell, MA: Kluwer, 2002). He holds several U.S. patents.

Dr. Wang is a Technical Program Committee member and session chairman for the IEEE Custom Integrated Circuit Conference (CICC 2001–2002). He is an AdCom member of the IEEE Electron Devices Society and a Distinguished Lecturer of the IEEE Solid-State Society. He is a frequent seminar speaker for both industrial and academic forums.